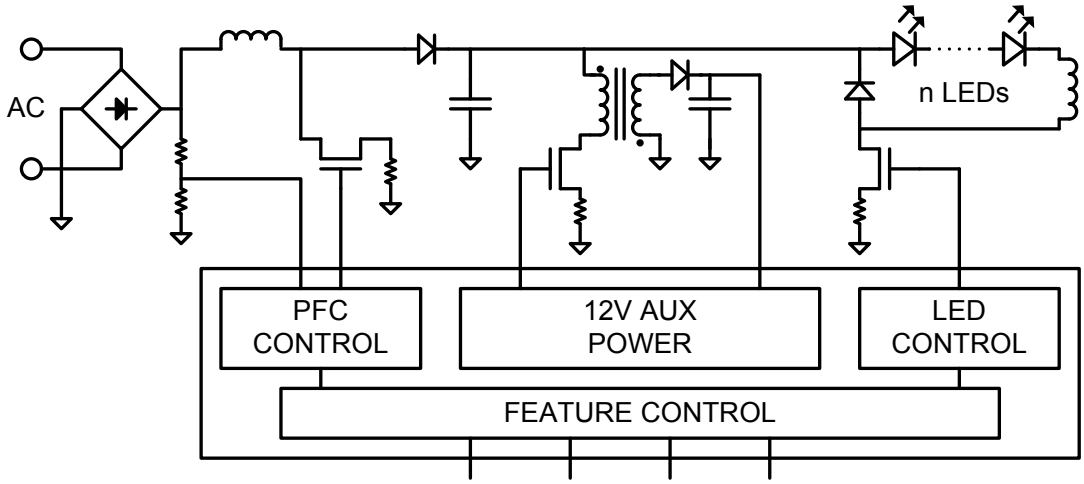
AC DIMMER COMPATIBLE LED CONTROLLER

- **Compatible With AC Dimmers**
- **Auxiliary Power Output: 12 V**
  - **200 mW When LED Is Off**
- **128 to 1 Brightness Control Via**
  - **AC Conduction Modulation, or**
  - **External Conduction Signal**
- **Local Brightness Setting**
  - **U / D Push Button Inputs**
  - **10 to 1 Range**
  - **14 Logarithmic Steps**
- **PFC for AC Input: PF > 0.95**
- **Built-In MOSFET Drivers**
- **Two ON / OFF Modes**
  - **Toggle and Closure**
  - **Built-In 3-Way Switch**
- **Smooth ON / OFF Transition**
- **LED Over Temp. Protection**
  - **Reduce Brightness > T_{LIMIT}**
  - **Continuous Light Output**
- **Direct LED Modulation**



The 908 / 909 products combine key features for intelligent, AC-powered LED lighting systems. Integrated into a 4x4 QFN package is power factor correction, triac dimmer compatibility, 128:1 brightness control, thermal management for long LED life, simple user interface for local brightness and on/off control, and auxiliary power for communication and sensor peripherals that is always available whether the LED is on or off.

The block diagram above shows the three key system blocks that are essential for intelligent lighting control systems: Power Factor Correction (PFC), LED Brightness Control, and Gate Drive / Auxiliary Power Generation.

The PFC circuit uses a resonance boost topology for zero current switching. The control loop is all digital, so only the output filter capacitor needs to be sized correctly. Feedback is through a resistor divider network that feeds internal analog-to-digital-to-analog control circuitry.

Power factor correction (PFC) is very important in applications that are widely deployed in large commercial and industrial settings. Although individual lighting fixtures may consume only 12 watts and may not be required to exhibit a high power factor, the deployment of thousands of fixtures with poor power factor correction can result in a poor power factor for the overall lighting system and increase the operating cost of the building.

Intelligent lighting systems usually include a communications channel and sensors for ambient light, motion, and self-diagnostics. These functions must be operational and independent of the LED light output. The 12 volt auxiliary power section provides this independent power though a flyback topology. The output is used to power the 908 / 909 part and other circuitry that does

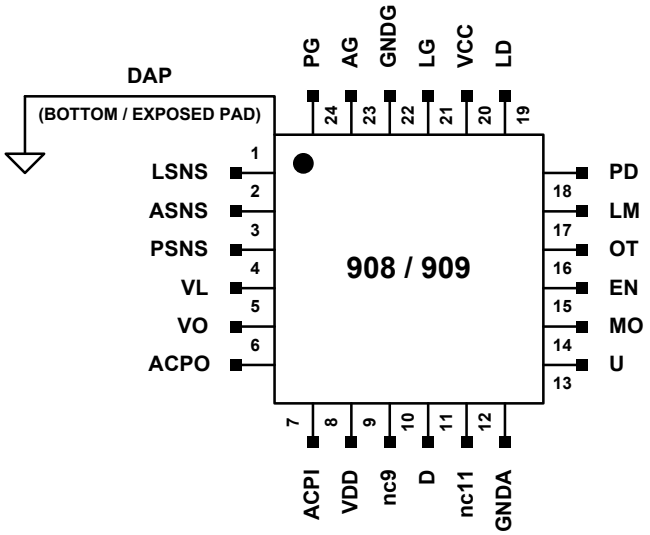
#	PIN	DESCRIPTION
1	LSNS	LED Source Sense
2	ASNS	AUX / Bias Source Sense
3	PSNS	PFC Source Sense
4	VL	AC Line Sense
5	VO	AC Voltage Sense
6	ACPO	AC Phase Output (low)
7	ACPI	AC Phase Input (low)
8	VDD	Regulated 5V
9	nc9	Do Not Connect
10	D	Decrease Brightness (low)
11	nc11	Do Not Connect
12	GNDA	Reference Return
13	U	Increase Brightness (low)
14	MO	Toggle ON / OFF (low)
15	EN	Enable ON (low)
16	OT	Over Temperature Sense
17	LM	LED Modulation (low)
18	PD	PFC Drain Sense
19	LD	LED Drain Sense
20	VCC	Supply (12V)
21	LG	LED Gate Drive
22	GNDG	Supply / Gate Return
23	AG	AUX / Bias Gate Drive
24	PG	PFC Gate Drive
-	DAP	Supply / Gate Return

not require isolation from the line voltage. Additional windings on the transformer can be used to generate coarse isolated voltages.

The difference between the 908 and the 909 is the control of the 12 volt auxiliary power section. The 908 keeps the auxiliary section always operational, even when the part is disabled through either the EN or MO pin. The 908 consumes approximately 3 mA at 12 volts when it is disabled. The auxiliary power section continuously supplies power to the 908 and peripheral circuitry.

The 909 shuts off the auxiliary power section when the part is disabled through either the EN or MO pin. This reduces the 909 current consumption to less than 500 µA. The 909 is intended for applications where very low "OFF" power is required. When VCC is isolated by a diode from external circuitry and battery power is used to backup VDD, the 909 typically consumes less than 50 µA.

The LED control section uses a buck topology to provide constant current drive to the LED. The LED brightness is controlled over a 128 to 1 range by pulse width modulation (PWM) at 244 Hz. The 908 / 909 product features multiple inputs to control the LED brightness.



908 Electrical Characteristics

Tj=25C, VCC = 12.0 V

Parameter	Test Condition	Symbol	Min	Typ	Max	Units
Operating						
VCC Supply Input		**VCC**	4		18	V
VDD Regulator Output	VCC > 8, part enabled	**VDD**		5.3		V
	VCC = 4, part enabled	**VDD**		VCC-0.3		V
	VCC > 8, part enabled with 5 mA load applied to VDD pin	**VDD**	4.4			V
VDD Capacitance	Bypass / Load capacitance at VDD	**CVCC**	100			nF
VCC ON Current	8 < VCC < 18, EN = L, CLoad = 1nF (LG, PG, AG)	**IVCC**			8	mA
VCC OFF Current	909 only, VCC = 4, EN = H	**IVCC**			500	µA
VDD OFF Current	909 only, VDD < 3 volts, VDD-0.5 ≤ VCC ≤ VDD, EN = H	**IVDD**		20		µA
Thermal Resistance	Junction to exposed pad	**θ_{JC}**	--	12	--	C/W
Junction Temperature	Degraded performance below -20 and above 90	**Tj**	-40	25	110	C
PFC						
VO regulation point		**VO**	0.97	1	1.03	Volts
VO lower limit	VOLL / VO	**VOLL**	0.915	0.933	0.95	
VO upper limit	VOUL / VO	**VOUL**	1.05	1.067	1.08	
Time Period	Design Range	**PFtp**	0.5		27	µsec
Charge Time (on)	Design Range	**PFtc**	0.3		13.3	µsec
Leading Edge Blanking		**PFtb**	55	70	90	nsec
Fault time		**PFtf**	210	250	290	nsec
Fault period		**PFtfp**	108	128	148	µsec
Sense threshold	PSNS, VL = 1.0, nom	**PFs**		500		mV
PD offset	PD - VO, VO = 1V	**PDoff**	-25	0	25	mV
12V Auxiliary Power (VCC)						
VCC start point	AG switching	**VCCs**		4		Volts
PFC start point	PG switching	**PFCs**		8		Volts
VCC regulation point		**VCC**		12		Volts
Time Period	Design Range	**APtp**	13.6	16	18.4	µsec
Charge Time (on)	Design Range	**APtc**	0.22		0.49*APtp	µsec
Leading Edge Blanking		**APtb**	55	70	90	nsec
Fault time		**APtf**		188	216	nsec
Fault period		**APtfp**	108	128	148	µsec
Sense threshold	ASNS	**APs**	170	200	230	mV

908 Electrical Characteristics

Tj=25C, VCC = 12.0 V

Parameter	Test Condition	Symbol	Min	Typ	Max	Units
LED Buck Converter						
Time Period	Design Range	**Btp**	0.65	4	13.6	µsec
Charge Time (on)	Design Range	**Btc**	0.216	--	12.8	µsec
Leading Edge Blanking		**Btb**	55	70	90	nsec
Fault time		**Btf**		188	216	nsec
Fault period		**Btfp**	218	256		µsec
Sense threshold	LSNS	**Bs**	190	200	210	mV
LD offset	LD - VO, VO = 1V	**LDoff**	-25	0	25	mV
LED Brightness Modulator						
PWM Frequency	Effective at LED	**Lfp**	208	244	280	Hz
PWM Period	Effective at LED	**Ltp**	--	4.1	--	msec
U/D Min Brightness	Effective at LED	**LUDmin**		384		µsec
ACPI Min Brightness	ACPI pulsed low, 0.03 < duty factor < 0.2	**LACmin**		32		µsec
ACPI Brightness duty	ACPI pulsed low for minimum brightness	**DACmin**			0.22	DF
	ACPI pulsed low for maximum brightness	**DACmax**	0.72			DF
ACPI Period	Design Range . Steady High = OFF	**TACmin**	4.7		13.9	msec
ACPI Brightness Hold	Max Brightness, Loss of AC line, ACPI = H	**TBHold**		49		msec
ACPI LED Shut-down	Max Brightness, Loss of AC line, ACPI = H	**TBoff**		197		msec
Hold Energy time	Design PFC output energy hold up time	**TEHold**		71		msec
OT Min Brightness	OT < OTRL	**LOTmin**		32		µsec
OT Update Period	OT < 0.139 * VDD	**TOT**		67		sec
LM Min pulse width	LM min pulse high.	**Ltmin**		32		µsec
Analog						
OT High Ratio, Cold temperature indication	OT ratio to VDD	**OTRH**	0.176	0.185	0.194	VDD
OT Low Ratio, Hot temperature indication	OT ratio to VDD	**OTRL**	0.139	0.146	0.153	VDD
OT Hysteresis, Ratio	OT ratio to VDD	**OTHYST**		0.039		VDD
ACPO Dynamic Drive	ACPO = VDD - 1	**AC_IOH**	10			mA
	ACPO = 1 volt	**AC_IOL**	10			mA
VL Low Threshold	ACPO transition from Low to High	**VLL**	175	200	225	mV
VL High Threshold	ACPO transition from High to Low	**VLH**	100	120	150	mV
VL Hysteresis	VLH - VLL	**VLHYST**	62	80	98	mV

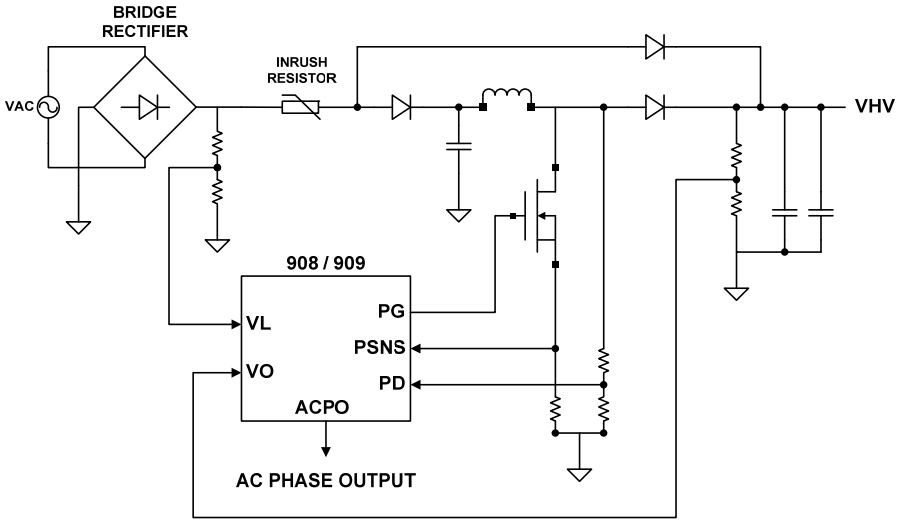
908 Electrical Characteristics

Tj=25C, VCC = 12.0 V

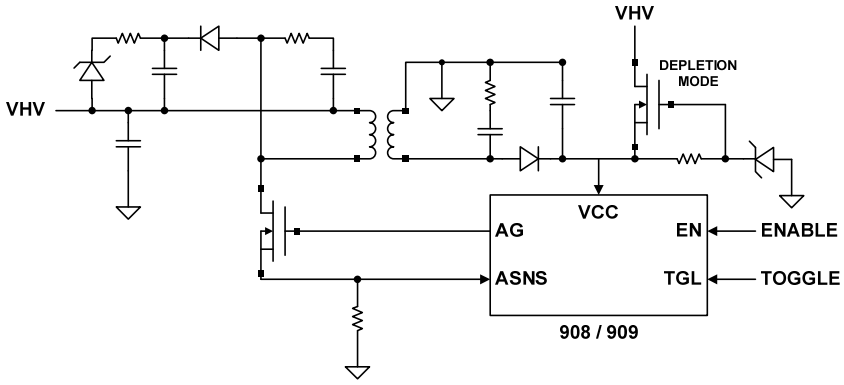
Parameter	Test Condition	Symbol	Min	Typ	Max	Units
External Gate Drive						
On Resistance LG, AG, PG	Output = LOW, IG = 100 mA, VCC = 12	**GNdson**		5		ohms
	Output = HIGH, IG = 100 mA, VCC = 12	**GPdson**		13		ohms
Digital						
EN (enable) threshold		**EN_L**		0.9		V
		EN_H		1.0		V
EN pull-up current		**EN_I**		1.0		µA
EN debounce		**EN_db**		40		msec
MO threshold		**MO_L**		0.9		V
		MO_H		1.0		V
MO pull-up current		**MO_L**		10.0		µA
MO debounce		**MO_db**		40		ms
U, D thresholds		**x_L**		0.9		V
		x_H		1.0		V
U, D pull-up current		**x_I**		10.0		µA
U, D Debounce		**x_db**		100		msec
LM thresholds		**LM_L**		0.9		V
		LM_H		1.0		V
LM pull-up current		**LM_I**		10.0		µA
ACPI thresholds		**AC_L**			0.3	VDD
		AC_H	0.7			VDD
ACPI input current		**AC_I**	-2		2	µA

FUNCTIONAL SCHEMATICS

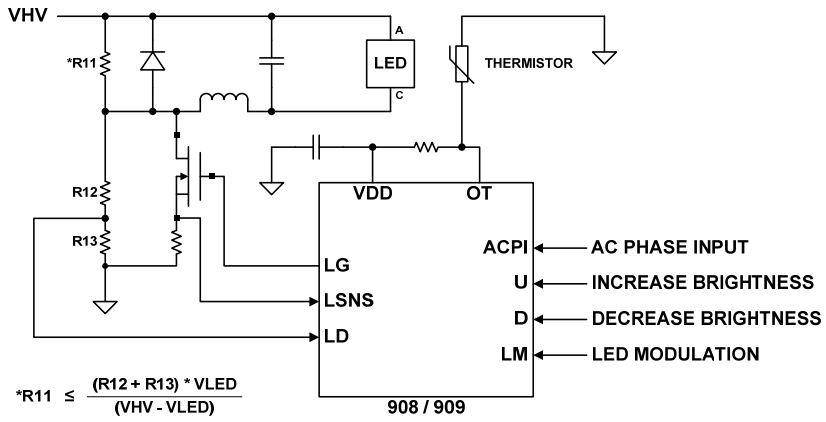
POWER FACTOR CORRECTION



12V AUXILIARY POWER / BIAS



LED BUCK CONVERTER



$$*R11 \leq \frac{(R12 + R13) * VLED}{(VHV - VLED)}$$

Operating Modes

Enabling the part is separate from enabling LED light output. The LED output is controlled by a conduction angle input (ACPI) (0% duty is off) and a direct modulation input (LM). The LM direct modulation input can be used for ON / OFF (signaling) as well as direct PWM brightness control.

There are two ways to enable the part: momentary contact closure (MO pin) and continuous contact closure (EN pin). Both MO and EN are active low with internal pull-up currents and have contact de-bouncing circuitry. The de-bouncing time is approximately 40 ms, which prevents inadvertent enabling.

EN enables the part when it is low and disables the part when it is high. MO acts as an electronic toggle switch to enable on the first activation and disable on the second activation. Note that MO can be used to disable the part when EN is low. If the part was enabled through MO, the EN pin can be used to disable the part by taking EN low and then high.

Enabling and disabling the part does not clear the last brightness setting. Only removal of power from the VCC pin and discharging the voltage at VDD to less than 10 mV for more than 10 ms assures a reset to full brightness. This protects the users setting from momentary AC line power losses and can be used in backup topologies to protect the user's setting for an indefinite amount of time.

LED brightness

There are 56 brightness settings that provide a control range of 128 to 1:

- Full brightness (100% LED duty)
- Minimum brightness (0.78% LED duty)
- Brightness steps are near logarithmic
- Brightness doubles or decreases by half for every 8 steps.

The LED PWM modulation rate is approximately 244 Hz and uses digital signal processing to create smooth transitions across the brightness range. When enabling the part at full brightness, the brightness will ramp from minimum to maximum brightness over approximately 10 power line cycles. When disabling the part, the brightness will ramp down for approximately 130 ms before the LED is shut off. This gives the effect of an incandescent bulb warming-up and cooling down and is easier on human eyes. (If a strobe effect is desired, the LM pin should be used to strobe the LED.)

Digital inputs U and D allow a user to increase or decrease the LED brightness over a 10 to 1 range with simple push button switches. Holding U or D active (low) will cause auto stepping of the brightness; this is similar to the volume control of audio products. The U/D input doubles/halves the brightness every four steps. By default the brightness setting starts at full brightness. This is the first level of control, which is followed by the ACPI and OT control inputs. The OT only limits brightness when an over temperature condition exists.

The conduction angle input (ACPI) can be used independently of the AC line waveform to control the brightness. Using optical isolators to modulate the ACPI input is the preferred way to control the brightness of multiple fixtures operating from different AC lines.

The ACPI input adjusts the brightness by sensing the duty factor of the low frequency input signal and mapping that duty factor to a logarithmic brightness value over a 128 to 1 range. When the duty factor is 0 (always high), the LED is off while other features of the 908 / 909 continue to be operational. A PWM signal with a repetition period between 5 and 13 ms will turn the LED on with the brightness determined by the duty factor of the PWM signal. When the duty factor (active low) is less than 0.22, the LED is at minimum brightness. When the duty factor is above 0.72, the LED is at full brightness. Between these two extremes, the brightness follows a near logarithmic path from less than 1% to 100% brightness.

The ACPI input can be used in conjunction with the ACPO output. The ACPO signal is a digital output with a duty factor that reflects the conduction angle from the triac dimmer. (See PFC section.) Together these signals produce a brightness setting that nearly matches the brightness variation of an incandescent bulb when con-

nected to a triac dimmer.

The direct modulation input (LM) causes the LED brightness to switch between off and the current brightness setting. This can be useful in situations where signaling or strobe effects are required. Also, LM can be used for direct brightness control through an external PWM source if ACPI is held low and neither D or OT have reduced the brightness. The LM signal can range from dc to 32 µs pulses. The LED is "ON" when the LM signal is at a logic HIGH level. If it is not used, it should be tied to the VDD pin.

The U and D inputs place a limit on the maximum brightness that the ACPI input can set. The ACPI input then operates within this brightness limit. The OT input will further reduc the brightness if the LED temperature has exceeded its upper limit as set by the OT input. The resultant brightness is a PWM signal that is sent to the LED output driver. Consequently, the LM signal, which directly modulates the LED output driver, will modulate with the resultant brightness PWM signal from the U, D, ACPI and OT inputs.

Over Temperature

The OT input is used to protect the LED from extreme operating temperatures. It senses the temperature of the LED with a thermistor (e.g. Murata NCP15WF104F03RC) to GNDA (pin 12). External resistors set the maximum LED operational temperature by adjusting the ratio from VDD to the OT input. Internal to the 908 / 909 is a resistor divider from VDD to the OT reference. An over temperature condition is sensed when the external ratio is less than 0.146. A "cool" condition is sensed when the external ratio is greater than 0.185. If the OT input is not used, it should be connected to VDD.

The OT input is periodically sampled to determine if the brightness of the LED needs to be reduced to correct an over temperature condition. If the LED temperature drops to a "cool" condition, the LED brightness limit is slowly increased in smooth transitions. The combination of hysteresis and digital control allows for very sensitive temperature control without oscillation in the brightness of the LED.

Power Factor Correction

The power factor correction circuit uses a resonance boost topology to increase the line voltage to a desired dc output voltage, VH. The 908 / 909 provides a nominal 12 volt gate drive to an external power FET that charges the input inductor. The current flowing through the inductor and FET is sensed by an external resistor at the source of the FET. The limit for the instantaneous current flow is determined by the rectified AC line voltage. Once this limit is reached, the FET is turned off and the inductor discharges to the output. When the inductor has fully discharged the FET is turned on again for another cycle. The current flowing through the AC line is approximately 1/2 the peak inductor current, which follows the input line voltage, and appears as a resistive load.

The control loop for the PFC is all digital with the exception of the output filter capacitor. The minimum output capacitor must be large enough that there is less than 3% ripple at the output under all input voltage and output load conditions. The VL input senses the rectified AC line voltage and sets the reference for the inductor current. The PSNS input senses the inductor charging current. Under nominal conditions, the peak input to VL is 1 volt and the peak sense voltage at PSNS is 0.5 volts. The output voltage is sensed through a resistor divider to the VO pin. The VO regulation point is 1 volt.

When the average voltage at VO is less than 1 volt, the inductor reference current is increased by increasing the scale factor from VL to PSNS. This increases the average input power. Conversely, when the average voltage at VO is greater than 1 volt, the scale factor is reduced and decreases the average input power. Through this action, the output voltage is regulated within a +/- 7% band around the regulation point as sensed by the VO pin.

The +/- 7% band is the limit of "normal" operation. If the output voltage is more than 7% above its regulation point, the boost converter is disabled until the output is within 7% of its regulation point. If the output voltage is less than 7% below its regulation point, the inductor current is rapidly increased until the output is back to the "normal"

operating range. In normal operation, the closed loop bandwidth is very low relative to the AC line frequency. The dominant source of ripple is the second harmonic current from the rectified AC line. The choice of the output capacitor is important for both low frequency ripple and the high frequency ripple from the PFC boost converter and LED buck converter.

The maximum inductor current is determined by the maximum voltage that can appear at the VL pin (rectified AC line voltage through a resistor divider) and the digital scale factor used to set the threshold at the PSNS input. The digital circuitry can use a maximum scale factor of 1 between the VL and PSNS pins.

Conversely, the minimum charge time is determined when the digital circuitry uses the minimum scale factor of 1/4 between VL and PSNS.

The digital logic has fault detection circuitry. If the charge time is too short, the logic will enter a fault state and force a 128 us discharge period. The minimum charge time should be greater than 300 ns to avoid accidental faulting of the control logic.

The charge time for the inductor is constant for a given power setting since the inductor charge current is proportional to the input voltage. However, the discharge time is longest at the peak of the AC line voltage.

T_{charge} = [I/V] * [Scale Factor] * L

Note I/V is constant for PF = 1

The discharge of the PFC inductor is sensed through a resistor divider from the power FET drain to the PD input. The PD input is compared to the VO input to determine when the inductor has discharged. When the inductor is fully discharged, the voltage at the drain will begin to ring around the instantaneous voltage of the rectified AC line voltage. A typical design ratio for the PD resistor divider network will set the PD input equal to the VO input when the drain voltage is slightly above the peak rectified AC line voltage.

The capacitance of the resistor divider network, traces, and input capacitance to the part require a capacitive divider in parallel with the resistor divider to minimize the signal delay from the drain of the power FET to the PD input. This capacitor divider network will become extremely important if an oscilloscope probe is occasionally placed on the PD pin.

The VL input pin also serves the purpose of creating the ACPO output signal. Fixed thresholds of approximately 0.12 and 0.20 volts are used to convert the voltage at VL into a digital signal that can be used for LED brightness control.

At low power requirement the PFC logic will use adaptive pulse period omissions to reduce the input power. Up to 7 PFC inductor cycles can be omitted when the lowest input power settings are used.

The PFC section will be disabled when the part is disabled with EN or MO. The PFC section will also be disabled if the ACPI input is held high for approximately 50ms. It is immediately re-enabled when the ACPI input transitions low. This reduces power when the LED has been shut off through the ACPI input or the part has been disabled. Note that LM does not affect the PFC operation.

12V Auxiliary / Bias Power

The integrated auxiliary power controller generates a low voltage supply that is independent of LED operation. This can provide the power for continuous command, control, and communication with the lighting resource and its sensors while the LED is off.

The 908 and 909 differ in the way the auxiliary power is managed. The 908 always generates the auxiliary power when more than 4 volts is applied to the VCC pin. The 909 only generates auxiliary power when enabled through either the EN or MO pin.

A flyback topology with a fixed 16 µs time period and fixed transformer current is used to generate a nominal 12 volts at VCC. An external FET charges the primary of the transformer during the first half of the period. The transformer secondary is discharged during the remaining time into the VCC circuit. The voltage at the VCC pin is used to determine whether another charge / dis-

charge cycle of the transformer is needed. This makes for a very simple and stable control system without additional feedback loop components. The output filter capacitor size is chosen for the required ripple at VCC. Ripple and regulation at VCC are not critical, since its primary purpose is to provide the gate drive voltage. Multiple windings of any ratio can be added to the transformer to provide multiple-isolated outputs.

Within the 908 / 909 product is a series regulator that generates approximately 5 volts at the VDD pin. This voltage is used by the internal analog and digital circuitry. At least 100 nF of capacitance is required for filtering at the VDD pin.

The Auxiliary power section needs to have at least 4 volts on VCC to start. This can be supplied by an external depletion mode FET, or resistor / capacitive divider to VCC . (The maximum voltage on VCC can not exceed 18 volts.) Once VCC is above 4 volts, the auxiliary power section will start and bootstrap VCC to 12 volts. When VCC is above 8 volts, the PFC section can start.

The AG pin supplies the gate drive for the external power FET. The threshold for this FET must be less than 4 volts for the bootstrap process to work. Current is sensed with a resistor at the source of the FET and is the input to the ASNS pin. When the voltage at the ASNS pin is above 200 mV, the AG pin is set low.

The maximum charge time is 1/2 the period. The minimum charge time is 220 ns. If the charge time of the transformer primary is less than 220 ns, then the period is extended to 128 us.

LED Buck Converter

The 908 / 909 combines a buck regulator with a PWM brightness circuit to manage the LED brightness. The buck regulator is designed to operate near boundary conduction mode. (Also referred to as borderline or critical conduction mode.) The full-brightness LED current is approximately one-half the peak inductor current. An output capacitor filters the inductor current so the LED load "sees" the average inductor current. Large capacitors are not necessary since the buck converter operates well above 60 KHz.

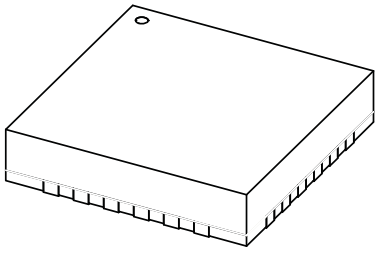
The control loop for the buck regulator is digital. The inductor is charged to twice the LED current and then discharged each cycle. The drain voltage of the external FET is sensed through a divider to the LD pin. The LD input is compared with the PFC output voltage sense input, VO, to determine when the inductor has discharged and when to start the next charging cycle. A typical design ratio for the LD resistor divider network will set the LD input equal to the VO input when the drain voltage is below the PFC output, VH, by the lowest expected LED voltage drop.

The capacitance of the resistor divider network, traces, and input capacitance to the part require a capacitive divider in parallel with the resistor divider to minimize signal delay from the drain of the power FET to the LD input. This capacitor divider network will become extremely important if an oscilloscope probe is occasionally placed on the LD pin.

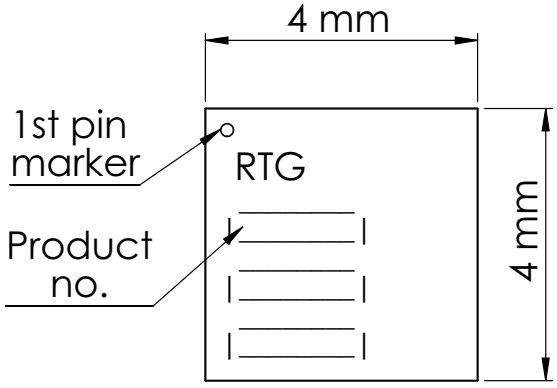
Only one external current sense resistor is required to set the full brightness of the LEDs. The inductor value, LED voltage, and PFC output voltage control the operating frequency of the regulator. The longest period is 16 µs (~60KHz). The longest charge time is 15 µs, followed by 1 µs off time. The shortest charge time is 220 ns. With typical discharge times less than 4 µs, this provides a very wide range of operating conditions and component values. This also simplifies the design process to selecting values for one resistor, one inductor, and the output capacitor for stable operation. Inductance values that increase the time period beyond 8 µs should be avoided since this may interact with the LED PWM brightness control at lowest brightness settings.

The LED buck circuit also protects against a shorted inductor / LED load by monitoring the charge time. If the set-current is reached in less than 220 ns, the circuit enters a fault mode to force the buck period to 256 µs until the fault is cleared.

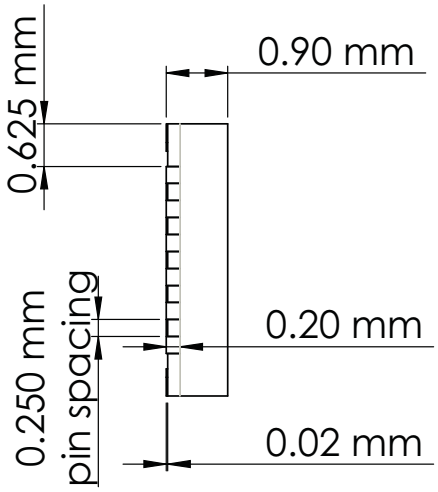
QFN—4X4—24 ld



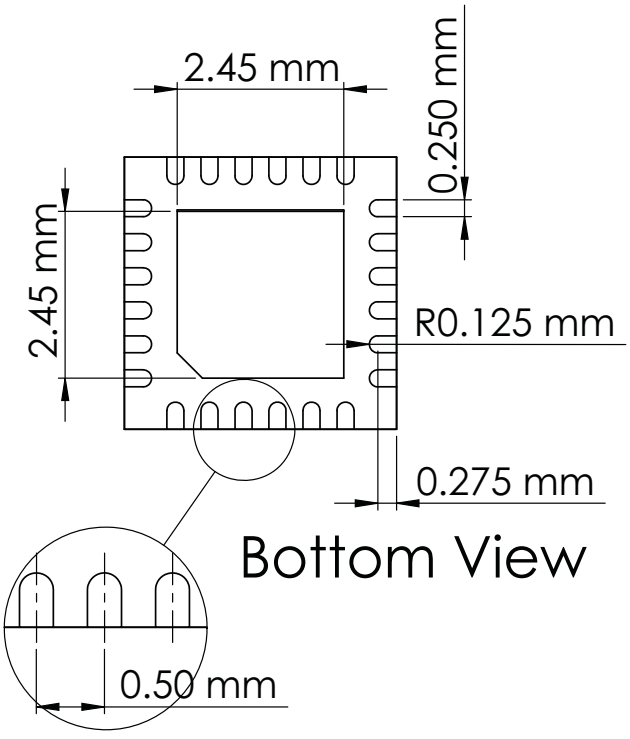
Trimetric View
6 pins per side



Top View



Side View



Bottom View

Detail C
Pitch